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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,521	02/09/2004	Sam Nemazie	SiliconStor-02US	1050

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EXAMINER	
LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,521	NEMAZIE, SAM	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-43 have been considered but are moot in view of the new ground(s) of rejection. Currently, claims 1-43 are pending for examination.

Terminal Disclaimer

2. The terminal disclaimer filed on 07/10/2006 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any patent granted on Application Numbers 10/775,488 and 10/775,523 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 6-14, 18-19, 23-32 and 36-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA:

the reality of Serial and Parallel ATA - Serial ATA", and further in view of Talati (US Patent 6,763,402).

4. As per claims 1, 18 and 31, Grieff teaches a switch coupled between a plurality of host units and a device via serial advanced technology attachment (SATA) for communicating there between and said switch comprising:

a) a first SATA port (Fig. 1, ref. 130) for connection to a first host unit, said first port for causing access, to the device, by the first host unit (col. 3, ll. 13-24 and col. 5, l.17 to col. 7, l. 6);

b) a second SATA port (Fig. 1, ref. 132) for connection to a second host unit, said second port for causing access to the device, by the second host unit (col. 3, ll. 13-24 and col. 5, l.17 to col. 7, l. 6);

c) a third SATA port (device-side link layer on Fig. 1) for connection to a device, for causing access to the device, by the first or second host units (col. 3, ll. 13-24 and col. 5, l.17 to col. 7, l. 6); and

d) an arbitration and control circuit (arbiter module 112 and switch 110 of Fig. 1), coupled to the first, second and third ports, for selecting one of the first host unit or the second host unit to be coupled to the device, through the switch (col. 3, ll. 13-24 and col. 5, l.17 to col. 7, l. 6).

Grieff does not expressly teach the switch comprising:

wherein the third port is a PATA port;

selecting one of the first host or the second host units to concurrently access the device by accepting commands, from either of the first or the second host units, at any given time, including when the deice is not in an idle state; and

wherein while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends ATA commands to the switch for execution by the device.

"SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" teaches the utilization of PATA ("SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", pages 1-2).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA's utilization of the PATA into Grieff's switch. The resulting combination of the references teaches the switch comprising of a third PATA port connecting to a peripheral device.

Therefore, it would have been obvious to combine "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" with Grieff for the benefit of having a peripheral port that is backward comparable allowing users to be able to connecting existing PATA peripheral devices instead of purchasing new peripheral devices that conform to the new SATA standard.

Talati teaches a system and a method comprising two or more hosts to simultaneous concurrent access the same data storage device by buffering any access request to the data storage device in a queue while said data storage device is busy

responding to a prior access and responded to the buffered access request later (col. 2, ll. 14-26).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Talati's queuing of access request into Grieff and SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA's arbitration and control circuit. The resulting combination of the references further teaches the switch comprising:

the first host unit and the second host unit to simultaneous concurrent access the device by buffering any commands received from either of the first host unit and the second host unit in the queue if the device is currently busy responding to the previous command, therefore able to accept the commands at any given time; and

wherein while the device is busy with the command from one of the first host unit or the second host unit, the other one of the first host unit or the second host unit sends the command to the switch for execution by the device as said command is buffered in the queue.

Therefore, it would have been obvious to combine Talati with Grieff and SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA for the benefit of preventing chaos that might occur in performing the concurrent access to the same storage device (Talati, col. 2, ll. 27-37).

5. As per claims 6, 23 and 36, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati teach all the limitation of claims 1, 18 and 31 as

discussed above, where Grieff further teaches the switch comprising wherein said device is a storage unit (Grieff, col. 15, ll. 9-22).

6. As per claims 7, 24 and 37, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati teach all the limitation of claims 1, 18 and 31 as discussed above, where Grieff further teaches the switch comprising wherein said switch is employed in an enterprise system (Grieff, col. 15, ll. 9-22).

7. As per claims 8, 25 and 38, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati teach all the limitation of claims 1, 18 and 31 as discussed above, where Talati further teaches the switch wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units (Talati, col. 1, l. 7 to col. 2, l. 36).

8. As per claims 9, 26 and 39, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati teach all the limitation of claims 1, 18 and 31 as discussed above, where Grieff further teaches the switch comprising wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units (Grieff, col. 12, l. 60 to col. 14, l. 28).

9. As per claims 10, 27 and 40, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati teach all the limitation of claims 9, 26 and 39 as discussed above, where Grieff further teaches the switch comprising wherein the information is referred to as `identify drive response` (IDENTIFY DEVICE) (Grieff, col. 7, ll. 39-61).

10. As per claims 11, 28 and 41, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati teach all the limitation of claims 9, 26 and 39 as discussed above, where Grieff further teaches the switch comprising wherein the information is referred to as `Tag` (Grieff, col. 12, l. 60 to col. 14, l. 28).

11. As per claims 12, 29 and 42, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati teach all the limitation of claims 1, 18 and 31 as discussed above, where Grieff further teaches the switch comprising wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the switch and the information is modified by the switch prior to being received by the device such that modified information rather than the information is received by the device (Grieff, col. 5, l. 65 to col. 6, l. 56 and col. 10, l. 27 to col. 11, l. 36).

12. As per claims 13 and 43, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati teach all the limitation of claims 12 and 42 as discussed above, where Grieff further teaches the switch comprising wherein the information is referred to as `Tag` (Grieff, col. 5, l. 65 to col. 6, l. 56 and col. 10, l. 27 to col. 11, l. 36).

13. As per claim 14, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati teach all the limitation of claim 13 as discussed above, where Grieff further teaches the switch comprising wherein the arbitration and control circuit include a Tag/Sactive Mapping Circuit (Grieff, Command Tracker SM 114 of Fig. 1) for mapping the host tag to the device tag and inverse mapping for identifying a host (Grieff, col. 5, l. 65 to col. 6, l. 56; col. 10, l. 27 to col. 11, l. 36 and col. 12, l. 60 to col. 14, l. 28).

14. As per claims 19 and 32, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati teach all the limitation of claims 18 and 31 as discussed above, where Grieff further teaches the switch comprising wherein the switch is a serial ATA switch (Grieff, col. 3, l. 13 to col. 4, l. 4 and col. 5, l. 65 to col. 6, l. 56).

15. As per claim 30, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati teach all the limitation of claim 28 as discussed above, where

Grieff further teaches the switch comprising wherein the information is referred to as `Tag` (Grieff, col. 5, l. 65 to col. 6, l. 56 and col. 10, l. 27 to col. 11, l. 36).

16. Claims 2-4, 20-22 and 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813), "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati (US Patent 6,763,402), and further in view of Ng (US Patent 6,388,590).

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati teach all the limitations of claims 1, 18 and 31 as discussed above.

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati does not expressly teach the switch comprising wherein the ports include a task file.

Ng teaches the coupling an ATAPI task file (Fig. 3, ref. 72b, 72a) to a serial transceiver port (Fig. 3, ref. 62a, 62b, 64a, 64b).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Ng's task file into Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati's switch ports. The resulting combination of the references teaches the switch further comprising the task file for each of the respective ports.

Therefore, it would have been obvious to combine Ng with Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati for the benefit of enable operation of data transferring at faster rate (Ng, col. 2, ll. 27-50).

17. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813), "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Talati (US Patent 6,763,402) and Ng (US Patent 6,388,590), and further in view of Boucher et al. (US Patent 6,434,620).

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Talati and Ng teach all the limitations of claim 4 as discussed above, where Grieff further teaches the switch comprising wherein said first, second and third ports are operating at link layer (level 2 ports) (Grieff, Fig. 1).

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Talati and Ng does not expressly teach the switch comprising wherein said first, second and third ports are level 4 ports.

Boucher teaches a communication interface between a peripheral comprising the intelligent network interface card (INIC 50 of Fig. 1) and a host (Fig. 1, ref. 52) comprising a physical layer communication path (Fig. 1, ref. 57) and two other communication paths at higher communication layer (Fig. 1 and col. 6, l. 60 to col. 7, l. 10).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Boucher's higher layer communication path into Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Talati and Ng's switch. The resulting combination of the references teaches the switch further comprising the ports, interconnection between the hosts and the peripheral device,

operating at level 4, as it is well known to one skilled in the art that the highest communication layer for SATA is application layer (level 4).

Therefore, it would have been obvious to combine Boucher with Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Talati and Ng for the benefit of providing a faster communication path between the peripheral device and the host (Boucher, Fig. 1).

18. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813), "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati (US Patent 6,763,402), and further in view of "Serial ATA Specification".

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati teach all the limitations of claim 1 as discussed above.

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati does not expressly teach the switch comprising wherein either the first or the second host sends a legacy queue command queued by the device; and wherein either the first or the second host sends a native queue command for execution thereof by the device.

"Serial ATA Specification" teaches the utilization of the legacy ATA queuing (legacy queue command) and the native Serial ATA queuing (native queue command) by the Serial ATA device (Section D.1.5 on page 301).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Serial ATA Specification's queuing of legacy queuing command and the execution of the native queuing command into Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati's switch.

Therefore, it would have been obvious to combine Serial ATA Specification with Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati for the benefit of because Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati's storage device conforms to the Serial ATA standard, therefore enable backward compatibility to prior technology standard and improve performance by enabling multiple commands to be outstanding within the SATA device at the same time.

19. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813), "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati (US Patent 6,763,402), and further in view of Boucher et al. (US Patent 6,434,620).

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati teach all the limitations of claim 1 as discussed above, where Grieff further teaches the switch comprising:

wherein said first, second and third ports are operating at link layer (level 2 ports) (Grieff, Fig. 1); and

a Data FIS FIFO (Grieff, host FIS buffer 120 and device FIS buffer 122 of Fig. 1) and an associated FIFO Control (Grieff, Command Tracker SM 114 of Fig. 1) are coupled to the first, second and third ports and are located externally thereto (Grieff, Fig. 1 and col. 5, l. 65 to col. 6, l. 56).

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati does not expressly teach the switch comprising wherein the first, second and third ports are level 3 SATA ports.

Boucher teaches a communication interface between a peripheral comprising the intelligent network interface card (INIC 50 of Fig. 1) and a host (Fig. 1, ref. 52) comprising a physical layer communication path (Fig. 1, ref. 57) and two other communication paths at higher communication layer (Fig. 1 and col. 6, l. 60 to col. 5, l.10).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Boucher's higher layer communication path into Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati's switch. The resulting combination of the references teaches the switch further comprising the ports, interconnection between the hosts and the peripheral device, operating at level 3, as it is well known to one skilled in the art that SATA standard comprise of four communication layers and one of said communication layer comprise of transport layer (level 3).

Therefore, it would have been obvious to combine Boucher with Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" and Talati for the benefit of

providing a faster communication path between the peripheral device and the host (Boucher, Fig. 1).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C.K.L.
08/30/2006

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SUPERVISORY PATENT EXAMINER
9/1/06